

Notice of References Cited

Application/Control No.

09/818,888

Applicant(s)/Patent Under

Reexamination

KIM, DONG-YUN

Examiner

Mark Connolly

Art Unit

2115

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-4,615,005	09-1986	Maejima et al.	713/601
	B	US-5,426,755	06-1995	Yokouchi et al.	711/101
	C	US-5,454,114	09-1995	Yach et al.	713/330
	D	US-5,907,699	05-1999	Nakajima, Toyokatsu	713/501
	E	US-6,044,282	03-2000	Hlasny, Daryl James	455/574
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 06332583 A	12-1994	Japan	YOSHIDA, YUKIHIRO	G06F 01/26
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Victor Nelson et al., Digital Logic Circuit Analysis and Design, 1995, Prentice-Hall Inc., pages 449-460.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.